ABSTRACT OF THE DISCLOSURE

A high speed operating circuit such as a data processor chip and memory chips constituting an electronic circuit is mounted to a multilayer wiring substrate in the state of a bare chip, and is set to a multichip module. This multichip module is mounted to a wiring substrate constituting the electronic circuit. In the multichip module, buffer circuits are inserted into a module internal bus commonly connected to the data processor chip and the memory chips. The buffer circuits are set to an address output buffer, a control signal output buffer and a data input/output buffer set to a high impedance state in accordance with an operating selection of the memory chips. When high frequency noise resisting characteristics are strengthened by the multilayer wiring substrate and the data processor chip gets access to the memory chips, an external noise tends to flow into a memory through the module internal bus connected to the data processor chip and the memory chips. However, the buffer circuits restrain the flow-in of such an external noise and prevent memory data from being broken by the high frequency noise during a memory access operation.